IN THE CLAIMS

Amend the claims as follows:

We claim:

1.(Amended) A parallel databus assembly, comprising:

a plurality of parallel signal lines;

a plurality of assemblies connected to said plurality of parallel signal lines, each of said assemblies having

a databus driver being in immediate connection with said signal lines, and

a controller connected to said databus driver,

at least some of said plurality of parallel signal lines being at least one of data lines for transmitting data and control lines for controlling data transmission of the data via said data lines,

a clock generator generating a predetermined bus frequency with which signals transmitted in said signal lines are clocked,

said databus drivers being connected to said clock generator, said databus drivers being fashioned such that signals to be transmitted from and to said data lines and said control lines are accepted during a clock pulse prescribed by said clock generator and are emitted during a following clock pulse.

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2. (Amended) A parallel databus assembly according to claim 1, wherein said clock generator generates a bus frequency of at least 20 MHz.

3. (Amended) A parallel databus assembly according to claim 2, wherein said clock generator generates a bus frequency of approximately 40 MHz

4. (Amended) A parallel databus assembly according to claim 1, wherein said databus has 32 data lines.

5. (Amended) A parallel databus assembly according to claim 1, wherein further ones of said plurality of parallel signal lines are fashioned as decision lines for deciding which of said plurality of assemblies connected to said parallel signal lines has access priority, and

said databus drivers having non-clocked open-drain outputs connected to said decision lines a wired-or logic is formed.

6. (Amended) A parallel databus assembly according to claim 5, further comprising:

a device for generating an auxiliary clock pulse with a lower frequency than the bus frequency is provided for driving the decision lines.

7. (Amended) A parallel databus assembly according to claim 6, wherein said device for generating an auxiliary clock pulse is a frequency divider.

8. (Amended) A parallel databus assembly according to claim 1, wherein outputs of the databus driver leading to the controller are fashioned as low-voltage TTL outputs.

9. (Amended) A parallel databus assembly according to claim 1, wherein said signal lines have a physical expanse of at least 40 cm.

10. (Amended) A parallel databus assembly according to claim 1, wherein said signal lines have a physical expanse of at least 50 cm.

11. (Amended) A parallel databus assembly according to claim 1, further comprising:

a processor for a plurality of the assemblies that are connected to the signal lines .

12. (Amended) A parallel databus assembly according to claim 1, wherein said databus is multibus-compatible.

13. (Amended) A method for communication of two assemblies which are each connected to a processor by a parallel databus, comprising the steps of:

exchanging data packets between the two assemblies; and

acknowledging each data packet by only one single handshake.

14. (Amended) A method according to claim 13, wherein said handshake includes a data-ready signal of the transmitter assembly and a data-ready signal of the receiver assembly, the data-ready signal of the transmitter assembly being sent to the receiver assembly at a beginning of the data transfer, and the receiver assembly sending a data-ready signal to the receiver assembly after the data-ready signal of the transmitter assembly has been received.

15. (Amended) A method according to claim 14, wherein said transmitter assembly only sends its data-ready signal when a complete data packet is present on said assembly.

16. (Amended) A method according to claim 14, further comprising the

step of:

setting a maximum size of the data packets to a predetermined value, and only sending a data-ready signal from the receiver assembly when there is sufficient storage space on the receiver assembly.

17. (Amended) A method according to claim 16, wherein said step of determining a maximum size determines one of 32 bytes and 64 bytes and 96 bytes and 128 bytes as the maximum size of the data packets.

18.(Amended) A printer control unit for high-performance printers, comprising:

an I/O-module,

at least one raster modules and

a serializer module,

a processor for each of said modules, and

a parallel databus.